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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,604	07/23/2004	Garth A. Brooks	BUR920040108US1	2285

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,604	BROOKS ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-30* is/are allowed.

6)☒ Claim(s) *1-8 and 11-18* is/are rejected.

7)☒ Claim(s) *9,10,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/23/04, 8/9/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0017675).

Re claims 1-4, Chen et al. disclose a method of fabricating a structure, comprising: forming a trench (204) in a substrate (200) (see Fig. 2C); depositing a first layer of polysilicon (216) on a surface of the substrate (200), the first layer of polysilicon (216) filling said trench (204) (see Fig. 2D); chemical-mechanical-polishing said first layer of polysilicon (216) at a first predetermined temperature to expose the surface of the substrate (see Fig. 2D and related text in Page 3, Paragraph [0028]); removing an upper portion of the first layer of polysilicon (216) from the trench (see Fig. 2E and related text in Page 3, Paragraph [0029]); depositing a second layer of polysilicon (224) on the surface of the substrate (200) (see Fig. 2G), the second layer of polysilicon (224) filling the trench; and chemical-mechanical-polishing the second layer of polysilicon at a predetermined second temperature to expose the surface of the substrate (200)

(see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Furthermore, the polishing temperature can be determined by routine optimization in order to control the uniformity of the CMP process.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to determine the polishing temperature since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed polishing temperature or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 5, as applied to claim 1 above, Chen et al. essentially disclose all the claimed limitations including the consecutive steps in order as recited in claim 1 (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Re claim 6, as applied to claim 1 above, Chen et al. disclose all the claimed limitations including doped first and second polysilicon. Furthermore, the claimed conductivity type, i.e., N-type is known in the art can be achieved by doping phosphors (P), arsenic (As) or other type of N-type dopant depending upon desirability and type of device. Hence, Examiner takes an

Official notice because it is well-known in the art form N-type polysilicon by doping the polysilicon using an N-type impurities such as phosphors (P), arsenic (As) or other type of N-type dopant depending upon desirability and type of device. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 7, as applied to claim 1 above, Chen et al. disclose all the claimed limitations including wherein said substrate includes an uppermost polishing stop layer; and forming of the trench comprises forming the trench through the polishing stop layer (i.e., pad layer **202**) (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Re claim 8, as applied to claim 1 above, Chen et al. disclose all the claimed limitations including forming the dielectric layer on the sidewall of the trench prior forming of the first polysilicon layer (see Fig. 2C and 2D) (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

3. Claims 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0017675) in view of Hieda et al. (US 5,998,821).

Re claim 11-14, Chen et al. disclose a method of fabricating a structure, comprising: forming a trench (204) in a substrate (200) (see Fig. 2C); depositing a first layer of polysilicon (216) on a surface of the substrate (200), the first layer of polysilicon (216) filling said trench (204) (see Fig. 2D); chemical-mechanical-polishing said first layer of polysilicon (216) at a first predetermined temperature to expose the surface of the substrate (see Fig. 2D and related text in Page 3, Paragraph [0028]); the first polysilicon in the trench dished at first distance form the bottom surface; removing an upper portion of the first layer of polysilicon (216) from the trench (see Fig. 2E and related text in Page 3, Paragraph [0029]); depositing a second layer of

polysilicon (224) on the surface of the substrate (200) (see Fig. 2G), the second layer of polysilicon (224) filling the trench; and chemical-mechanical-polishing the second layer of polysilicon at a predetermined second temperature to expose the surface of the substrate (200), the second polysilicon layer in the trench dished into the trench at second distance and the first distance grater than the second distance (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

However, Chen et al. do not specifically disclose the claimed CMP temperature range and plurality of trenches.

Hieda et al. disclose forming of array of trenches (see Fig. 2) and forming the fist polysilicon layer in the trenches dished from the bottom surface of the trench at a first distance; forming of a second polysilicon in the trenches over the fist polysilicon dished in the trenches at a second distance, wherein the first distance is greater than the second distance (see Figs. 2 –9B). Hieda et al. formation of array of trenches is desired to form the trench capacitor.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Chen et al. reference with array of trenches as taught by Hieda et al. because the trenches used to form trench capacitors.

Furthermore, the polishing temperature can be determined by routine optimization in order to control the uniformity of the CMP process.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to determine the polishing temperature since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Hoeschele*, 406 F.2d 1403,

160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed polishing temperature or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 15, as applied to claim 11 above, Chen et al. and Hieda et al. in combination disclose essentially disclose all the claimed limitations including the consecutive steps in order as recited in claim 1 (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Re claim 16, as applied to claim 11 above, Chen et al. and Hieda et al. in combination disclose all the claimed limitations including doped first and second polysilicon. Furthermore, the claimed conductivity type, i.e., N-type is known in the art can be achieved by doping phosphors (P), arsenic (As) or other type of N-type dopant depending upon desirability and type of device. Hence, Examiner takes an Official notice because it is well-known in the art form N-type polysilicon by doping the polysilicon using an N-type impurities such as phosphors (P), arsenic (As) or other type of N-type dopant depending upon desirability and type of device. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 17, as applied to claim 11 above, Chen et al. and Hieda et al. in combination disclose all the claimed limitations including wherein said substrate includes an uppermost

polishing stop layer; and forming of the trench comprises forming the trench through the polishing stop layer (i.e., pad layer **202**) (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Re claim 18, as applied to claim 11 above, Chen et al. and Hieda et al. in combination disclose all the claimed limitations including forming the dielectric layer on the sidewall of the trench prior forming of the first polysilicon layer (see Fig. 2C and 2D) (see Figs. 2C – 2G and related text in Page 2, Paragraph [0024] though Page 3, Paragraph [0031]).

Allowable Subject Matter

4. Claims 9, 10, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 10 and 20 are also objected as being dependent of claims 9 and 19.

5. Claims 21-30 are allowed over prior art of record.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach "forming a NFET in said substrate and adjacent to said trench, a source of said NFET in physical and electrical contact with said second layer of polysilicon in said trench," as recited in claim 21.

Claims 22-30 are also allowed as being directly or indirectly dependent of the allowed independent claim.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Sandhu et al. (US 5,196,353) disclose CMP process.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
August 4, 2006